CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the above-referenced application.

Listing of Claims:

Claims 1-14 (Cancelled)

15. (Previously presented) A delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising:

an inverter chain containing not less than four inverters;

a p-channel metal-oxide-semiconductor transistor and an n-channel metal-oxide-semiconductor transistor, known as MOS transistors, to comprise each of the at least four inverters, wherein a gate threshold voltage of each gate of said p-MOS and n-MOS transistors is shifted in mutually opposing directions;

low threshold voltage n-MOS transistors of each of a first and a third inverter connected to ground by a high threshold voltage n-MOS transistor; and

low threshold voltage p-MOS transistors of each of a second and a fourth inverter connected to a power source line by a high threshold voltage p-MOS transistor;

wherein, when an input logic signal is fixed at a low level during a standby state, said high threshold voltage n-MOS transistor is set to an off-state in response to a chip select signal controlling said standby state, and said high threshold voltage p-MOS transistor is set to an off-state in response to said chip select signal that is negated.

Claims 16-21 (Cancelled)

22. (Previously Presented) A delay circuit, comprising:

first, second and third nodes;

a first inverter, the output of which coupled to said first node, and first inverter receiving a logic signal;

a second inverter, the input of which coupled to said first node and the output of which coupled to said second node;

a third inverter, the input of which coupled to said second node and the output of which coupled to said third node;

a fourth inverter, the input of which coupled to said third node,

wherein at least one of said inverters includes a pair of transistors, a gate threshold voltage of each gate of said pair of transistors being shifted in mutually opposing directions;

a first capacitor having two electrodes, one of said electrodes connecting to a first power source line and the other connecting with a wiring layer having both ends to said first node, said wiring layer having no connection with a circuit at any points thereon between said both ends, said first capacitor being a first transistor of a first channel type;

a second capacitor coupled between said third node and said first power source line, said second capacitor being a second transistor of said first channel type; and

wherein no capacitor is connected to said second node.

23. (Previously presented) A delay circuit according to claim 22, wherein said first transistor and said second transistor are p-MOS transistors, and said first power source line is fixed at a power potential.

24. (Previously presented) A delay circuit according to claim 22, wherein said first transistor and said second transistor are n-MOS transistors, and said first power source line is fixed at a ground potential.

Claims 25 - 28 (Cancelled)

29. (Previously Presented) A delay circuit, comprising:

2n+1 nodes defined in series, n being a natural number, a first node receiving a logical signal;

2n inverters, each inverter arranged between adjacent nodes of said 2n+1 nodes, wherein at least one of said inverters includes a pair of transistors, a gate threshold voltage of each gate of said pair of transistors being shifted in mutually opposing directions;

a capacitor of an n-MOS type coupled between an even node and a power source line; and

a NOR gate coupled to the first node and the (2n+1)th node.

Claims 30 and 31 (Cancelled)

32. (Previously Presented) A delay circuit receiving a logic signal having a first logical level and a second logical level, comprising:

a first inverter chain including a plurality of inverters and at least one first capacitor, said first inverter chain receiving said logic signal and said first capacitor including a MOS transistor of a first channel type,

wherein said first capacitor changes from an off-state to an on-state to increase capacitance thereof when said logic signal changes from said first logical level to said second logical level, whereby said first inverter chain outputs a first delay signal generated after a first delay time from a transition timing from said first to said second logical levels of said logic signal, and

wherein said first capacitor changes from said on-state to said off-state to decrease capacitance thereof when said logic signal changes from said second logical level to said first logical level, whereby said first inverter chain outputs a second delay signal generated after a second delay time from a transition timing from said second to said first logical levels of said logic signal, said second delay time being shorter than said first delay time;

a first logical gate receiving the output of said first inverter chain and said logic signal;

a second inverter chain including a plurality of inverters and at least one second capacitor, said inverter chain receiving the output of said first logical gate;

a second logical gate receiving the output of said first logical gate and the output of said second inverter chain; and

a third logical gate receiving said logic signal and the output of said second logical gate,

wherein at least one inverter in said first and second inverter chains includes a pair of transistors, a gate threshold voltage of each gate of said pair of transistors being shifted in mutually opposing directions, and wherein said first inverter chain and said second inverter chain have the same structure.